Digital IF Implementation of the GSM and EDGE Modulation/Demodulation Schemes on the same Hardware Platform

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Abstract --This paper illustrates that the software radio principles are of great interest in the context of multi-standard environments. Taking advantage of last generation VLIW DSPs and configurable DUC/DDC, waveforms are generated at Tx and processed at Rx, in the digital domain, using the same HW components. In software radio as much as possible of the processing is done in software. Our case study is a real-time dual mode GSM-EDGE modulation/demodulation IF testbed. The functional mapping of the SW blocks on the HW platform and its performance are described.

Index Terms--Software Radio, multi-mode, digital IF, dual mode GSM/EDGE, VLIW DSP, undersampling...

I. INTRODUCTION

Dual mode radio systems are currently most of the time made of the juxtaposition of two physical hardware chains integrated in the same box. In these transceiver chains, architecture commonality stops at the point that the digital signal processing accelerates. In most present designs specific analog circuitry handles frequency up-conversion from baseband (BB) for Tx and down-conversion to baseband for Rx. The extension of the digital processing closer to the antenna, in other words replacing the former analog processing, permits to use of the same components and contributes to bring more and more re-configurability to the radio part. Digital often indeed means configurable.

This paper gives a concrete illustration of these assessments in the context of a dual mode GSM-EDGE system, combining that way both voice and high data rate services. Only modulation and demodulation functions are concerned here, from baseband to a low IF of several MHz. In the following, after presenting the generic platform used as a proof of concept for SoftWare Radio (SWR) implementations, we describe in detail the dual GSM-EDGE modem implementation. Finally, performance, in terms of signal quality and processing speed, is discussed.

II. A SWR EXPERIMENTATION PLATFORM

A. General description

In our laboratory an experimentation platform was assembled to study SWR system design, as well as reconfigurability and reconfiguration issues [1].

This platform, shown in FIG. 1, has a modular hardware architecture making future upgrades possible. The presence of multiple DSPs enables the study of multiprocessing issues. In the future the introduction of FPGA modules will permit to apply co-design techniques and address hardware and software reconfiguration in a unified manner. A/D and D/A boards interface the digital part to the air medium, enabling digital IF applications. All code development is done in C offering a high degree of portability from this platform to any other processor, as SWR dogma requires. Finally, taking advantage of the universal decomposition of any radio signal by its quadrature components, a complex representation of any baseband signal is possible.

B. Detailed Tx

The SWR approach consists in moving the digital
to analog conversion (DAC) as close as possible to the antenna. Frequency translation can be done digitally by multiplication of the I and Q data streams (DDS: Direct Digital Synthesis) as shown on FIG. 2.

\[ \text{Pulse shaping} \rightarrow \hat{x}(t) \rightarrow \text{Over sampling} \rightarrow \text{DAC} \]

FIG. 2 – Functional diagram of the digital transmitter

The physical architecture of the transmit part of our platform is depicted in FIG. 3; it is appropriate to implement the functionality of FIG. 2. Note that the DDS function may be realized either by the digital upconverter (DUC) chip or by DSP software when the DUC is by-passed.

FIG. 3 – Platform transmitter

C. Detailed Rx

To adhere to the software radio design philosophy, a wideband RF sampling ADC replaces the multiple front ends. A top-level functional block diagram of such a digital receiver is shown in FIG. 4.

FIG. 4 – Functional diagram of the digital transmitter

This has been realized on the hardware (HW) system of FIG. 5. The digital down converter (DDC) is by-passable.

FIG. 5 – Platform receiver

III. SW IMPLEMENTATION

The implementation is described below. Though our performance target was 270.83 kbauds (as defined in the standards), the following examples have been worked out for a symbol rate of 250 kbauds for simplification and ease of understanding.

A. GSM

FIG. 6 and 7 represent the functional block diagram of the GSM modulator and demodulator.

FIG. 6 - GSM functional block diagram for Tx

FIG. 7 - GSM functional block diagram for Rx

B. EDGE

EDGE [2] functional block diagram of the transceiver is on FIG. 8 and 9.

FIG. 8 - EDGE functional block diagram for Tx
It is worth noting that an important part of Rx functionality is synchronization (carrier recovery and sampling time adjustment). These functions were implemented as well but are not shown to keep the figures simple.

The mapping operation on the HW results in the characteristics of TAB 1.

<table>
<thead>
<tr>
<th></th>
<th>GSM</th>
<th>GSM</th>
<th>EDGE</th>
<th>EDGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{DAC}}$ (kbits/s)</td>
<td>250</td>
<td>250</td>
<td>750</td>
<td>750</td>
</tr>
<tr>
<td>$f_{\text{symbols}}$ (ksymbols/s)</td>
<td>250</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>BB oversampling</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>$f_{\text{samples}}$ (Msamples/s)</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>DAC interpolation</td>
<td>8</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{\text{DAC}}$ (MHz)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>decimation</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>$f_{\text{DAC}}$ (MHz)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>$f_0$ (MHz)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>IF (MHz)</td>
<td>10</td>
<td>10</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

**TAB. 1 - GSM and EDGE transceivers**

**C. Undersampling**

It can be seen that in the GSM case we use the undersampling technique. At Tx, the goal is to produce sampled versions of the modulated signal by using a sampling rate $f_{\text{DAC}}$ greater than $2 f_0$, where $f_0$ is a low carrier frequency. Taking advantage of the replicas of the digital signal the real carrier frequency IF is chosen at $n f_{\text{DAC}}+f_0$ where $n$ is a positive integer. Similarly at Rx, a convenient ratio between IF and $f_{\text{samples}}$ has to be respected [3].

**IV. PERFORMANCES**

Performance is considered both in terms of quality of the transmitted signal, and of computation speed of the software running on the DSP processor.

**A. Measured quality with a VSA**

The modulators were validated using a vector signal analyzer (VSA), and the results shown in FIG. 10 were obtained for EDGE.

**FIG. 10 - EDGE for $f_{\text{RF}} = 2$ MHz**

**Error Vector Magnitude (EVM) figures of TAB. 2 reveal quite satisfactory. EVM gives the deviation of a received constellation from an ideal reference constellation.**

**TAB. 2 - Error vector magnitude (EVM)**

<table>
<thead>
<tr>
<th>Modulation</th>
<th>RF</th>
<th>EVM (% rms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>2 MHz</td>
<td>1.24</td>
</tr>
<tr>
<td></td>
<td>10 MHz</td>
<td>2.32</td>
</tr>
<tr>
<td>EDGE</td>
<td>2 MHz</td>
<td>0.159</td>
</tr>
</tbody>
</table>

**B. Implemented performances**

Several performance measurements were obtained. Performance was considered in terms of execution speed (CPU cycle counts) and attained bit rates. The results are given in TAB. 3. For the two implementation schemes, we measured the global performance of the Tx, Rx chains as well as the performance of only the modem functionality.

**TAB. 3 - Attained bit rates for GSM and EDGE**

It can be seen that for single processor implementations (C6201 DSP at 200 MHz) of Tx, Rx for GSM, EDGE the attained performance is higher than the required for one channel. The C6x roadmap shows that soon processors at 1GHz clock speeds will be available (i.e. C64x). Having the software written in
high-level language code will permit to easily take advantage of technological progress in processor design and manufacturing. The present measurements indicate that a single C6x could handle both Tx, Rx at the same time and deliver real-time performance.

However it must be noted that currently the C6x DSP chip is not destined to mobile terminals due to its high power consumption, size and price.

C. Repartition of the computation load

Another set of measurements investigates how processing time is distributed among the transceiver functional blocks, as shown in FIG. 11.

In the GSM Tx implementation the \( \cos, \sin \) calculations are obtained by the CORDIC trigonometric algorithm [4]. Other more computationally efficient, tailored to the GMSK case, methods could be used. [5] combines gaussian filtering and cos, sin computations into table lookups and potentially it can be extremely fast. At the Rx CORDIC is used for angle (phase) computation using the \( \arctan \) function.

These comparative results confirm that modulators are a lot simpler than demodulators especially when carrier and timing recovery needs to be implemented. In addition it is clear that filtering for pulse shaping though a simple operation it is the most time consuming and this gets worse for higher oversampling factors. Such simple (regular) but time consuming processing is a good candidate for a more hardware oriented implementation. FPGA implementation is very promising in order to retain the flexibility offered by reprogrammability.

V. CONCLUSIONS

The results presented here show that it is now feasible to implement some kind of SWR by extending digital, and especially software, domain to at least some IF. In other words, it is possible to design a dual-mode GSM / EDGE, modulation / demodulation system running on exactly the same components.

What has been shown here for one 250 kHz channel is applicable in a multi-carrier situation, which we plan to study in the future. We have also applied the same concept to other wireless systems such as Bluetooth, and the future 3G cellular phone standard UMTS [6]. In these cases several processors have to be involved to obtain real-time performance.

However it should be noted that the components we used are not those found in current embedded or portable systems for size and energy consumption reasons. Also for the time and analog RF was ignored in our work. As technology progress in these directions the SWR concept will find its way in such applications as well.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

[5] GMSK modulator on DSP, article RF Design